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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,380	09/10/2003	Woo-Jong Lee	277/ 021	3327

7590 02/24/2006

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EXAMINER	
SCHINDLER, DAVID M	

ART UNIT	PAPER NUMBER
2862	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,380	LEE ET AL.	
	Examiner	Art Unit	
	David Schindler	2862	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-12,15 and 16* is/are allowed.

6)☒ Claim(s) *9,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Bot Ledynh
Primary Examiner

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication received on 12/08/2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Renger (5,764,052).

Renger discloses a pulse controller (32) for generating a pulse to block current from flowing into a driving coil (40) of the fluxgate before an end of a cycle of the sensing apparatus (Column 7, Lines 22-26) when it is determined that conversion of an analog signal from the fluxgate to a digital signal is completed by an A/D converter (48) and the A/D converter outputs the digital signal to the pulse controller ((Figures 1 and 4) and (Column 7, Lines 12-15) and (Column 7, Lines 22-26)).

Examiner is interpreting the end of the cycle of the sensing apparatus to be when the pulse controller (microprocessor / (32)) turns the transistor off (Column 7, Lines 22-25). It is noted that the outputting of the pulse to block current (low voltage level) must occur before transistor is turned off.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Renger (5,764,052).

As to Claim 9,

AAPA discloses a fluxgate (Figure 1) including a driving coil (40) for exciting a magnetic substance core with a current (Page 1, Paragraph [0003], Lines 2-3), first (30) and second (31) current amplifiers for applying the current to first and second ends of the driving coil (Page 1, Paragraph [0003], Lines 4-5), and a pulse generator (10) for generating a pulse to turn on/off the first and second current amplifiers (Page 2, Paragraph [0004], Lines 1-2).

AAPA does not disclose a pulse controller for outputting a control signal allowing the pulse to be applied to the first and second current amplifiers, the pulse controller outputting the control signal at a start of a sensing cycle, the fluxgate generating an analog signal due to the excited magnetic substance, and an A/D converter for converting the analog signal from the fluxgate into a digital signal, wherein the pulse controller stops outputting the control signal before an end of a cycle of the sensing apparatus when the A/D converter outputs the digital signal to the pulse controller.

Renger discloses a pulse controller (32) for outputting a control signal allowing a pulse generator (38) to apply a signal to a coil, the pulse controller outputting the control signal at a start of a sensing cycle (Column 6, Lines 7-11), the fluxgate generating an analog signal (Vout) due to the excited magnetic substance ((Column 3, Lines 56-57)

and (Column 6, Lines 53-63), and an A/D converter (48) for converting the analog signal from the fluxgate into a digital signal (Figure 1), wherein the pulse controller stops outputting the control signal before an end of a cycle of the sensing apparatus when the A/D converter outputs the digital signal to the pulse controller (Column 7, Lines 22-26).

It would have been obvious at the time of the invention to modify AAPA to include a pulse controller for outputting a control signal allowing the pulse to be applied to the first and second current amplifiers, the pulse controller outputting the control signal at a start of a sensing cycle, the fluxgate generating an analog signal due to the excited magnetic substance, and an A/D converter for converting the analog signal from the fluxgate into a digital signal, wherein the pulse controller stops outputting the control signal before an end of a cycle of the sensing apparatus when the A/D converter outputs the digital signal to the pulse controller given the above disclosure and teaching of Renger in order to measure an external magnetic field (Column 1, Line 62-63).

Examiner is interpreting the end of the sensing cycle to be when the pulse controller (microprocessor / (32)) turns the transistor off (Column 7, Lines 22-25). It is noted that pulse controller must stop outputting the control signal (logic high value / (Column 6, Lines 7-9)) before the transistor is turned off by the low level voltage (Column 7, Lines 22-25).

As to Claim 14,

AAPA discloses a driving coil (40) for exciting a magnetic substance core with current (Page 1, Paragraph [0003], Lines 2-3), first (30) and second (31) current amplifiers for applying current to first and second ends of the driving coil ((Figure 1) and

(Page 1, Paragraph [0003], Lines 4-5), and a fluxgate (Figure 1) with a pulse generator (10) for generating a pulse to turn on/off the first and second current amplifiers (Page 2, Paragraph [0004], Lines 1-2).

AAPA does not disclose an A/D converter for converting an analog signal from the fluxgate into a digital signal, and a pulse controller for outputting a control signal for controlling the pulse generator, the control method including a) driving the pulse generator when the fluxgate initiates a drive and outputting a first control signal in order for the pulse generated from the pulse generator to be applied to the first and second current amplifiers, and b) outputting a second control signal in order for the pulse generated from the pulse generator not to be applied to the first and second current amplifiers when the conversion of the analog signal into the digital signal by the A/D is complete before an end of a cycle of the sensing apparatus and the A/D converter outputs the digital signal to the pulse controller.

Renger discloses an A/D converter (48) for converting an analog signal from the fluxgate into a digital signal (Figure 1), and a pulse controller (32) for outputting a control signal for controlling the pulse generator (38), the control method including a) driving the pulse generator (38) when the fluxgate initiates a drive and outputting a first control signal in order for the pulse generated from the pulse generator to be applied to a coil ((Figures 1 and 4) and (Column 6, Lines 7-11)), and b) outputting a second control signal in order for the pulse generated from the pulse generator not to be applied to the coil when the conversion of the analog signal into the digital signal by the A/D is complete before an end of a cycle of the sensing apparatus and the A/D converter

outputs the digital signal to the pulse controller ((Figures 1 and 4) and (Column 7, Lines 12-30)).

It would have been obvious at the time of the invention to modify AAPA to include an A/D converter for converting an analog signal from the fluxgate into a digital signal, and a pulse controller for outputting a control signal for controlling the pulse generator, the control method including a) driving the pulse generator when the fluxgate initiates a drive and outputting a first control signal in order for the pulse generated from the pulse generator to be applied to the first and second current amplifiers, and b) outputting a second control signal in order for the pulse generated from the pulse generator not to be applied to the first and second current amplifiers when the conversion of the analog signal into the digital signal by the A/D is complete before an end of a cycle of the sensing apparatus and the A/D converter outputs the digital signal to the pulse controller given the above disclosure and teaching of Renger in order to measure an external magnetic field (Column 1, Line 62-63).

Examiner is interpreting the end of the sensing cycle to be when the pulse controller (microprocessor / (32)) turns the transistor off (Column 7, Lines 22-25). It is noted that the outputting of a second control signal (low voltage level) must occur before transistor is turned off.

Allowable Subject Matter

6. Claims 10-12, 15, and 16 are allowed.

7. The following is an examiner's statement of reasons for allowance:

As to Claim 10,

The primary reason for the allowance of claim 10 is the inclusion of an AND gate for logical AND-ing the pulse from the pulse generator with the control signal from the pulse controller and for outputting an output signal to the first and second current amplifiers in accordance with the logical AND-ing. It is these features found in the claim, as they are claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

As to Claim 15,,

The primary reason for the allowance of claim 15 is the inclusion of logical AND-ing the pulse from the pulse generator with the control signal from the pulse controller and outputting an output signal to the first and second current amplifiers in accordance with the logical AND-ing. It is these features found in the claim, as they are claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments filed 12/08/2005 that pertain to Claims 9, 13, and 14 have been fully considered but they are not persuasive.

Note: U.S. Patent Number 5,764,052 to Renger (herein referred to as "the Renger reference").

With regard to section B of pages 1-2 of Applicant's Remarks, Applicant's arguments are persuasive in combination with the currently amended Claims 9, 13, and 14, and as such the 112, first paragraph, rejection has been withdrawn.

With regard to Applicant's arguments in section D of pages 2-3 of Applicant's Remarks, the Examiner respectfully disagrees. First, Applicant argues that there is no control signal per se being output to be stopped, especially not before an end of a cycle of the sensing apparatus, as now recited in claim 13 (see lines 5-6 of the last paragraph of page 2 of Applicant's Remarks). The Examiner notes that in Column 6, Lines 7-11, the Renger reference states "...the microprocessor outputs a logic high value (at T0) to turn on the transistor 34. This causes the capacitor 38 to discharge through the transistor 34, inducing a current through ... the coil 40." In Column 7, Lines 22-26, the Renger reference states "Once Vout has been measured (using ... the A/D converter 48 ...), the microprocessor 32 switches the port POUT back to a low voltage level, turning off the transistor 34 and allowing the capacitor 38 to recharge (through the resistor 36)." Therefore, the Renger reference has two control signals (a logic high value and a low voltage level) and that once Vout has been measured using the A/D converter, the logic high value control signal is stopped and is no longer output, and a low voltage level is output instead. The Examiner further notes that the cycle of the sensing apparatus of the Renger reference has been interpreted to be when the pulse controller (microprocessor / (32)) turns the transistor off (Column 7, Lines 22-25). Therefore, the

logic high value control signal must be stopped and no longer output before the end of the cycle of the sensing apparatus so that the low voltage level control signal can be output and the transistor turned off.

Secondly, Applicant argues that any control signal in the Renger reference appears to be a time lapse trigger rather than an event trigger (see the last two lines of page 2 of Applicant's Remarks). The Examiner notes that neither a time lapse trigger nor an event trigger is claimed. Applicant additionally argues that the event trigger is clearly the A/D converter outputting the digital signal to the pulse controller (see lines 1-2 of page 3 of Applicant's Remarks). With regard to this argument, the Examiner notes the phrase in Column 7, Lines 22-26 of the Renger reference which states "Once Vout has been measured (using ... the A/D converter 48 ...), the microprocessor 32 switches the port POUT back to a low voltage level, turning off the transistor 34 and allowing the capacitor 38 to recharge (through the resistor 36)." It appears from the above phrase that the microprocessor does not switch the port POUT back to a low voltage level until Vout has been measured. Please see lines 12-26 of column 7 of the Renger reference and also note Figure 1 and the relationship between Vout, the A/D, and the microprocessor. The Examiner therefore respectfully disagrees with Applicant's argument's as the Renger reference appears to include the claimed limitations of Claim 13.

With regard to section E on page 3 of Applicant's Remarks, please see the above response with respect to section D of Applicant's Remarks.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Schindler whose telephone number is (571) 272-2112. The examiner can normally be reached on M-F (8:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Lefkowitz can be reached on (571) 272-2180. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Schindler
Examiner
Art Unit 2862

DS